REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 7, 2002, and the references cited therewith.

Claims 19, 20, 53, 79, 82, 85, and 107-112 are amended, as a result, claims 19, 20, 53, 79-87, 98-102, and 104-124 remain pending in this application.

§102 Rejection of the Claims

Claims 19, 53, 79, 81, 85, 87, 107, 111, and 112 were rejected under 35 USC § 102(e) as being anticipated by Azuma et al. (U.S. Patent No. 5,708,302).

Applicant makes no admission that the Azuma et al. patent constitutes prior art, and reserves the right to swear behind the Azuma et al. patent. Nevertheless, Applicant believes the claims are patentably distinct from the Azuma et al. patent for the reasons presented below.

Claim 19 recites a capacitor comprising a first conductive capacitor plate, a second conductive capacitor plate, and a dielectric interposed between said first and second conductive capacitor plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive capacitor plate. For clarity, claim 19 is amended to recite that the metal layer includes a "non-oxidized portion" and an "oxidized portion", wherein the "oxidized portion" is a dielectric of the capacitor.

Azuma et al. disclose, in FIG. 1, a first electrode 24 and a dielectric layer 26. In column 4, lines 55-58, Azuma et al. clearly state that electrode 24 is a combination of all of the layers 34, 36, 38, and 40. Thus, Azuma et al. disclose two distinct layers: electrode 24 (34, 36, 38, and 40) and dielectric 26. As shown in FIG. 1, dielectric 26 is not an "oxidized portion" of any metal layer. Therefore, Azuma et al. do not disclose a metal layer overlying the first conductive capacitor plate (electrode) in which the metal layer includes a "non-oxidized portion" and an "oxidized portion", wherein the "oxidized portion" is the dielectric of the capacitor.

Based on the reasons presented above, claim 19 is not anticipated by Azuma et al. Applicant requests that the rejection of claim 19 be reconsidered and withdrawn and that claim 19 and its dependent claims be allowed.

Claim 53 is amended. As amended, claim 53 recites elements similar to the elements of claim 19. As presented above, claim 19 is not anticipated by Azuma et al. Thus, claim 53 is also not anticipated by Azuma et al for reasons similar to the reasons presented about regarding claim 19. Applicant requests that the rejection of claim 53 be reconsidered and withdrawn and that claim 53 and its dependent claims be allowed.

§103 Rejection of the Claims

Claims 20, 82, 84, 109, and 110 were rejected under 35 USC § 103(a) as being unpatentable over Boldgett et al. (U.S. Patent No. 5,811,990) in view of Azuma et al.

Claim 20 recites a capacitor comprising a first conductive capacitor plate, a second conductive capacitor plate, and a dielectric interposed between said first and second conductive capacitor plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive capacitor plate. For clarity, claim 20 is amended to recite that the metal layer includes a "non-oxidized portion" and an "oxidized portion", wherein the "oxidized portion" is a dielectric of the capacitor.

Boldgett et al. do not disclose a metal layer including a "non-oxidized portion" and an "oxidized portion", wherein the "oxidized portion" is a dielectric of the capacitor. As presented above in the 102 section, Azuma et al. also do not disclose a metal layer overlying the first conductive capacitor plate in which the metal layer includes a "non-oxidized portion"and an "oxidized portion", wherein the dielectric is the "oxidized portion" of the capacitor. Thus, neither Boldgett et al. nor Azuma et al. disclose all of the elements of claim 20. Therefore, claim 20 is patentable over Boldgett et al. and Azuma et al. Applicant requests that the rejection of claim 20 be reconsidered and withdrawn and that claim 20 and its dependent claims be allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 7 day of February, 2003.

Tina Kohout
Name

Signature

Docket No. 303.455US3 Micron Ref. No. 95-0505.02
WD # 353042

CLEAN VERSION OF PENDING CLAIMS

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION
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Claims 19, 20, 53, 79-87, 98-102, and 104-124, as of February 7, 2003 (Date of Response to Final Office Action and RCE).

19. (Amended) A capacitor, comprising:

a first conductive capacitor plate of a first material;

a second conductive capacitor plate; and

a metal layer of a second material overlying the first conductive capacitor plate, wherein the metal layer includes a non-oxidized portion and an oxidized portion, wherein the oxidized portion is a dielectric of the capacitor.

20. (Amended) A memory system, comprising:

a monolithic memory device, comprising a capacitor, wherein the capacitor comprises:

a first conductive capacitor plate;

a second conductive capacitor plate; and

a metal layer of a second material overlying the first conductive capacitor plate, wherein the metal layer includes a non-oxidized portion and an oxidized portion, wherein the oxidized portion is a dielectric of the capacitor; and

a processor configured to access the monolithic memory device.

53. (Amended) A capacitor comprising:

a first capacitor electrode;

a metal layer overlying the first capacitor electrode, wherein the metal layer includes a non-oxidized portion and an oxidized portion, wherein the oxidized portion is a dielectric of the capacitor; and

G1 cont E2

a second capacitor electrode.

G1 E3

79. (Amended) The capacitor of claim 19, wherein the oxidized portion of the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

80. The capacitor of claim 79, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

81. The capacitor of claim 19, wherein the second conductive capacitor plate is formed from a material selected from the group consisting of polysilicon and metal.

G1 E4

82. (Amended) The memory system of claim 20, wherein the oxidized portion of the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

83. The memory system of claim 82, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

84. The memory system of claim 20, wherein the second conductive capacitor plate is formed from a material selected from the group consisting of polysilicon and metal.

G1 E5

85. (Amended) The capacitor of claim 53, wherein the oxidized portion of the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

86. The capacitor of claim 85, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

87. The capacitor of claim 53, wherein the second capacitor electrode is formed from a material selected from the group consisting of polysilicon and metal.

98. A capacitor formed by a process comprising:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose a portion of the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose an upper surface of the insulative layer;

depositing a metal layer to overly the polysilicon layer, the metal layer being formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer;

oxidizing at least a portion of the metal layer to form a metal oxide to function as a dielectric layer; and

forming an electrically conductive layer overlying the metal oxide.

99. The capacitor of claim 98, wherein the electrolytic solution is a basic solution.

100. The capacitor of claim 98, wherein the electrolytic solution is an acidic solution.

101. The capacitor of claim 98, wherein the electrolytic solution is a solution of one part NH_4OH to ten parts water.

102. The capacitor of claim 98, wherein the electrolytic solution is a 0.1 molar solution of $HClO_4$.

104. A capacitor, comprising:

a first conductive plate serving as a first electrode of the capacitor;

a second conductive plate serving as a second electrode of the capacitor, the second conductive plate formed from a material selected from the group consisting of polysilicon and metal; and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

105. A memory system, comprising:

a monolithic memory device comprising a capacitor, wherein the capacitor comprises

a first conductive capacitor plate,

a second conductive capacitor plate formed from a material selected from the group consisting of polysilicon and metal, and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead; and

a processor configured to access the monolithic memory device.

106. A capacitor comprising:

a first capacitor electrode comprising polysilicon;

a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead; and

a second capacitor electrode formed from a material selected from the group consisting of polysilicon and metal.

107. (Amended) The capacitor of claim 19, wherein the oxidized portion of the metal layer comprises titanium.

108. (Amended) The capacitor of claim 19, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the oxidized portion of the metal layer.

109. (Amended) The memory system of claim 20, wherein the oxidized portion of the metal layer comprises titanium.

110. (Amended) The memory system of claim 20, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the oxidized portion of the metal layer.

111. (Amended) The capacitor of claim 53, wherein the oxidized portion of the metal layer comprises titanium.

112. (Amended) The capacitor of claim 53, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the oxidized portion of the metal layer.

113. The capacitor of claim 104, wherein the first conductive plate comprises polysilicon having a thickness of 200 to 400 Angstroms.

114. The capacitor of claim 104, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

115. The memory system of claim 105, wherein the first conductive capacitor plate comprises polysilicon.

116. The memory system of claim 105, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

117. The capacitor of claim 106, wherein the first capacitor electrode has a thickness from 200 to 400 Angstroms.

118. The capacitor of claim 106, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the metal layer.

119. A capacitor structure formed on a substrate, comprising:

a first conductive capacitor plate formed atop the substrate;

a first metal layer formed atop the first conductive capacitor plate;

a first metal oxide layer formed from the metal layer such that the remaining first metal

layer forms part of the first conductive capacitor plate; and

a second conductive layer formed atop the first metal oxide layer.

120. The capacitor structure of claim 119, further including:

a second metal layer formed atop the second conductive layer;

a second metal oxide layer formed from the second metal layer such that the remaining second metal layer forms part of the second conductive layer;

a third conductive layer formed atop the second metal oxide layer, wherein the first and second metal oxide layers and the second conductive layer form the dielectric of the capacitor and the third conductive layer serves as a second conductive capacitor plate.

121. The capacitor structure of claim 119, wherein:

the first conductive capacitor plate comprises polysilicon and the first metal layer comprises a metal selected from the group of metals consisting of titanium, tungsten, copper, gold, and nickel.

122. The capacitor of claim 119, wherein the first metal layer is substantially completely oxidized to form the metal oxide layer.

123. The capacitor of claim 119, wherein the first metal oxide layer has a thickness of between 10 and 1000 Angstroms.

124. The capacitor of claim 119, wherein the first metal layer is alloyed with another material.